

LAB 3: - DECODERS, DISPLAYS AND MULTIPLEXERS

**ITI1100 - Digital Systèmes
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Objective

- Analyse, construct and test a simple 2-to-4 decoder.
- Construct and test a seven-segment decoder display
- Analyse, construct and test a simple multiplexer.

Equipment and components

- Quartus II 13.0 Service-Pack 1
- Altera DE2-115 card

Circuit Diagrams

Part I – A 2-to-4 Decoder

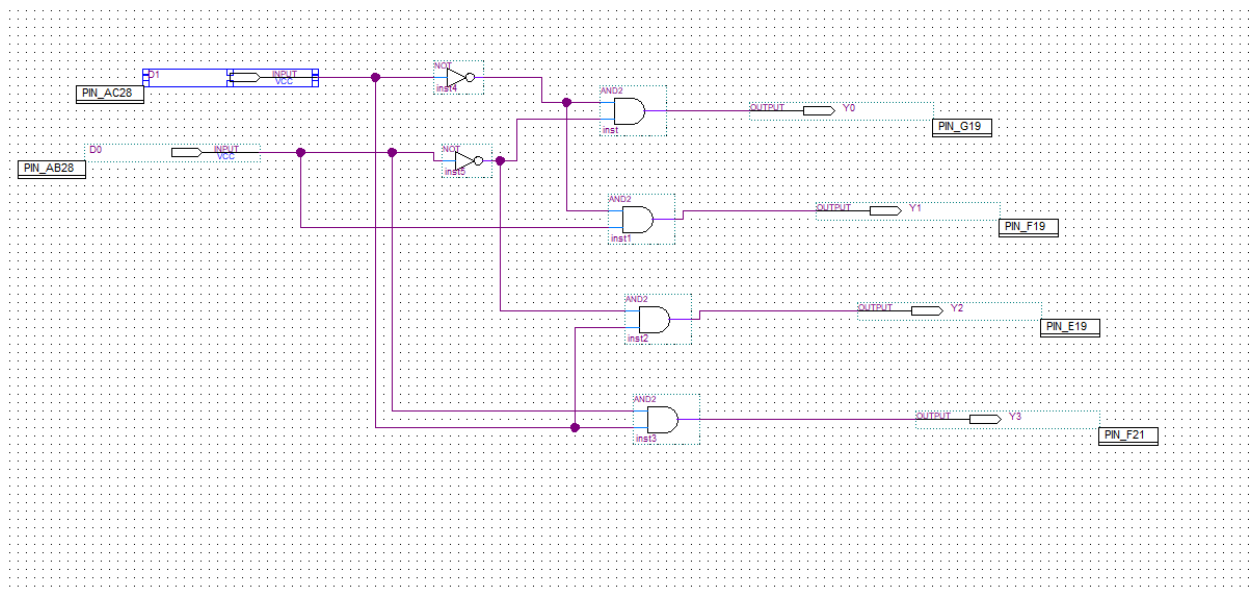


Figure 1: Screenshot of a circuit diagram of a 2 to 4 decoder (Figure 5.3.2 of the lab manual)

Part II – Decoder and Seven Segment Display

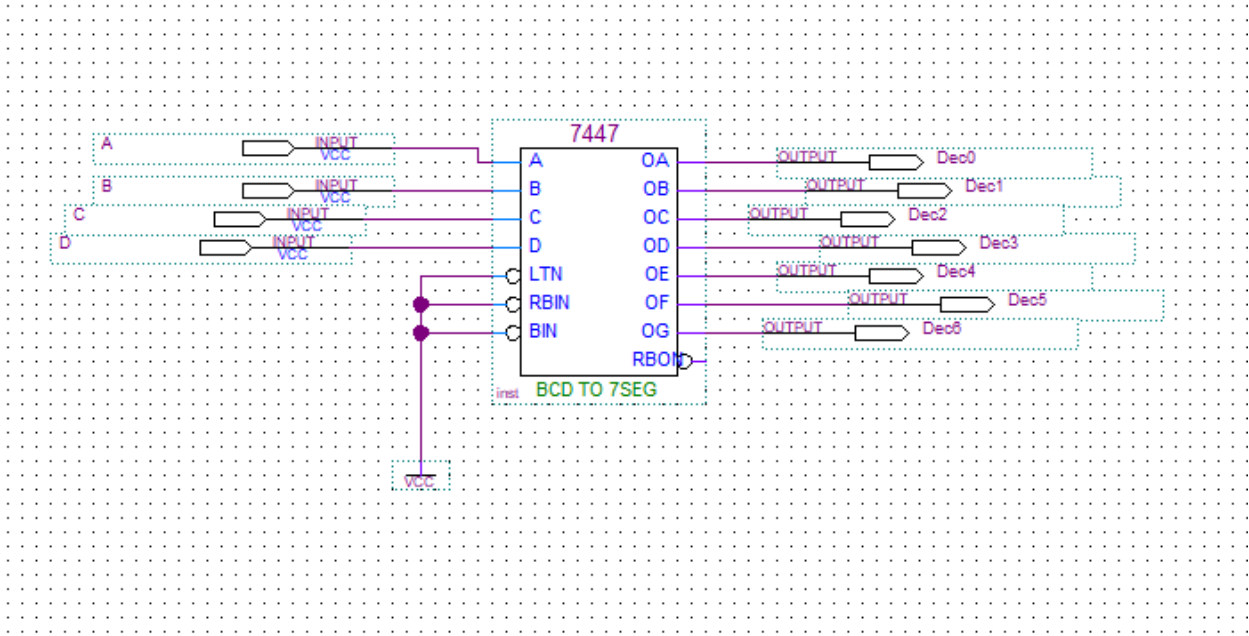


Figure 2: Screenshot of a circuit diagram of a standard decoder and circuit display for a 7-segment display (Figure 5.3.4 in the lab manual)

Part III – Multiplexers

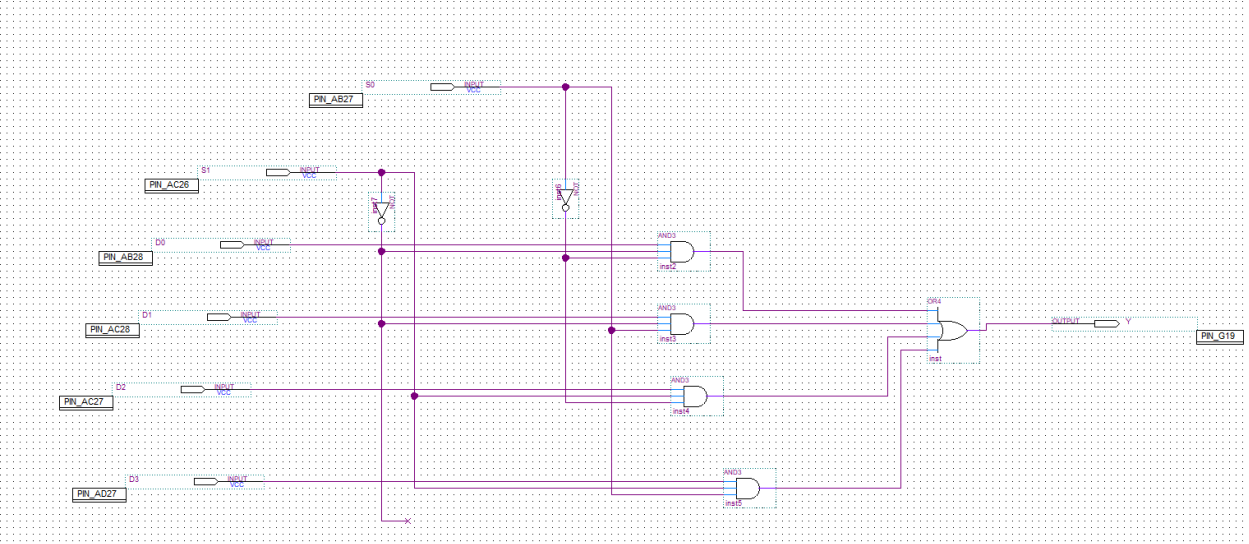
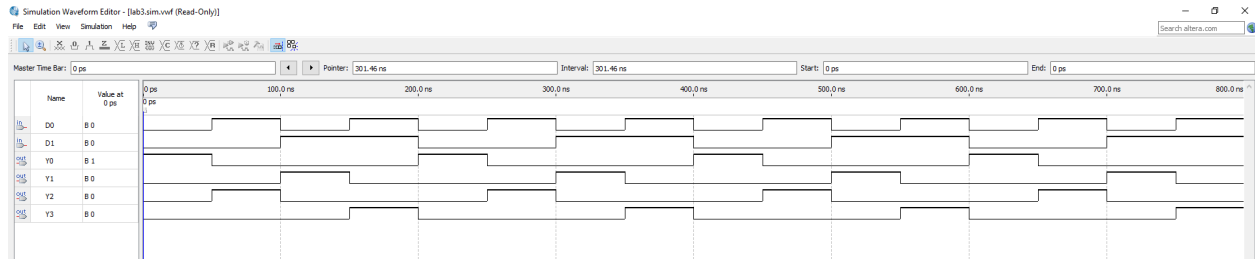


Figure 3: Screenshot of a schematic of a 4-in-1 multiplexer (Figure 5.3.5 in the manual of the laboratory)

Experimental Data and Data Processing

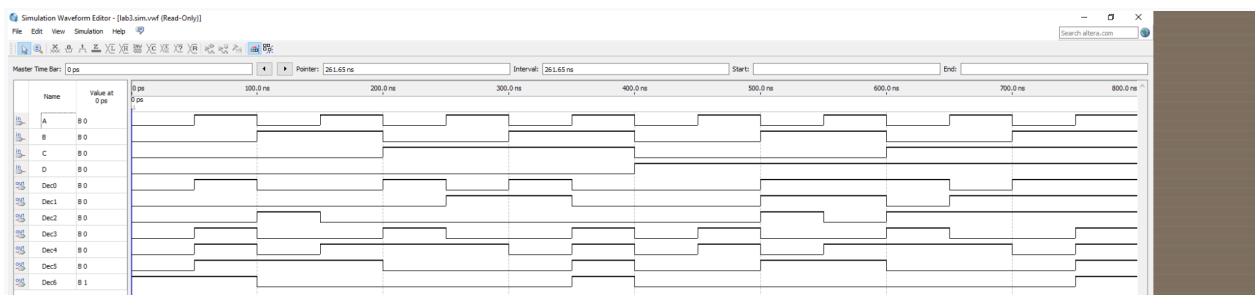
Part I – A 2-to-4 Decoder



Inputs determined from dip switches		Observed LED output			
D ₀	D ₁	Y ₀	Y ₁	Y ₂	Y ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 1: Experimental data observed from the circuit board in Figure 1

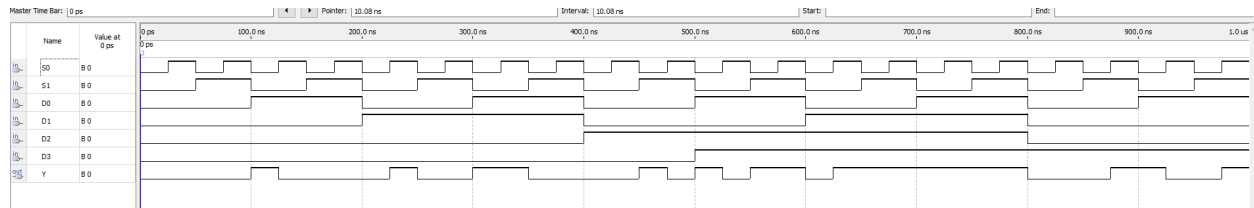
Part II – Decoder and Seven Segment Display



Inputs				Outputs						
A	B	C	D	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	0	1	0	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0

Table 2: Experimental data observed from the circuit board in Figure 2

Part III – Multiplexers



Inputs determined from DIP switches						Observed output of the LED
S ₀	S ₁	D ₀	D ₁	D ₂	D ₃	Y
0	0	0	x	x	x	0

0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Table 3: Experimental data observed from the PCB in Figure 3

Comparison of Theoretical Data and Experimental Data

Part I – A 2-to-4 Decoder

Table 1-2 : Comparison of Theoretical and Experimental results from *circuit diagram of a 2 to 4 decoder*

Inputs		Expected Results				Actual Results			
D ₀	D ₁	Y ₀	Y ₁	Y ₂	Y ₃	Y ₀	Y ₁	Y ₂	Y ₃
0	0	1	0	0	0	1	0	0	0
0	1	0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0	0	1

The results observed experimentally for a circuit of a 2 to 4 decoder were identical to the results obtained theoretically as expected

Part II – Decoder and Seven Segment Display

Table 5: Comparison of theoretical and experimental results for a circuit logic using two types of gates

Inputs				Expected Results						Expected Results							
A	B	C	D	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0
0	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0

The results observed experimentally for a circuit two types of gates were identical to the results obtained theoretically as expected

Table 5.3.1: Display corresponding to 0-9 digits

D ₃ D ₂ D ₁ D ₀	Corresponding Display	D ₃ D ₂ D ₁ D ₀	Corresponding Display
0000	0	0001	1
0010	2	0011	3

0100	4	0101	5
0110	6	0111	7
1000	8	1001	9

Part III – Multiplexers

Table 6: Comparison of theoretical and experimental results for a circuit logic using a 4-to-1 multiplexer circuit

Inputs						Expected Results	Actual Results
S ₀	S ₁	D ₀	D ₁	D ₂	D ₃	Y	Y
0	0	0	x	x	x	0	0
0	0	1	x	x	x	1	1
0	1	x	0	x	x	0	0
0	1	x	1	x	x	1	1
1	0	x	x	0	x	0	0
1	0	x	x	1	x	1	1
1	1	x	x	x	0	0	0
1	1	x	x	x	1	1	1

The experimentally observed results for a 4-to-1 multiplexer circuit were identical to the results obtained theoretically as expected

Discussion and conclusion:

Some minor hardware issues have caused a delay in completing the experiment, However, the experiment concluded with an expected results table and completely matching outcomes. Since we have only worked with small LEDs as the output technology so far, it was helpful in to demonstrate the same principles through another output. In particular, the 7-segment display proved to be a useful tool in showcasing numerous applications for binary numbers, as well as circuit patterns and other previously encountered technologies.

The decoder was another application of minimization and simplification. Using two variables to produce four unique results was more efficient than having one result per variable or a similar configuration. The concepts derived from executing this initial experiment can be applied to larger decoders to achieve exponentially larger result pools from relatively few input variables.

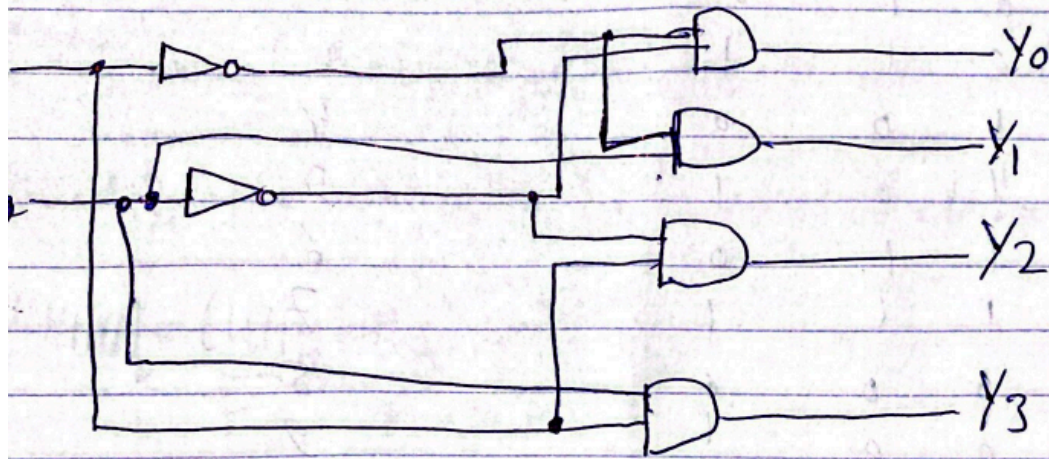
The use of the multiplexer explained the almost opposite effect compared to the decoder. Instead of using a number of variables to control even more output variables, the multiplexer was able to utilize switching variables to determine which data variables would affect the final output. In this way, different results could be obtained by considering different variables. In a project setting, this could translate to employing a different method to obtain a variable while still using it for the same result.

This lab demonstrates several ways to utilize variables for controlling one another, for different types of output, and for various output sizes. It serves as a valuable testament to the versatility of utilizing variables in any good system

Appendix (Pré-Lab)

Part ①:

$$Y_0 = \bar{D}_1 \bar{D}_0, \quad Y_1 = \bar{D}_1 D_0, \quad Y_2 = D_1 \bar{D}_0, \quad Y_3 = D_1 D_0$$



D_1	\bar{D}_1	D_0	\bar{D}_0	Y_0	Y_1	Y_2	Y_3
0	1	1	0	0	1	0	0
1	0	1	0	0	0	1	0
0	1	0	1	1	0	0	0
1	0	0	1	0	0	0	1

When $D_1 D_0 = 1$, so the output will always be Y_1 .

Part (2)

D_3	D_2	D_1	D_0	Corresponding Display
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Part (3)

It is 4 to 1 multiplexer.

$$Y = \bar{S}_1 \bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1 \bar{S}_0 D_2 + S_1 S_0 D_3$$

S_1	S_0	D_3	D_2	D_1	D_0	Y	
0	0				0	0	$Y = D_0$
0	0				1	1	
0	1			0			$Y = D_1$
0	1			1			
1	0		0				$Y = D_2$
1	0		1				
1	1	0					$Y = D_3$
1	1	1					